REMARKS

Claims 1, 3, 5-9, 11-16, 18-21, and 23-31 are pending.

Copies of the PTO Form 1449's filed on May 22, 2003 and September 16, 2004, along with date-stamped postcards evidencing the filings, are submitted herewith. Applicant respectfully requests that the Examiner consider the references cited therein and return the initialed PTO Form 1449's.

Rejections under 35 U.S.C. § 102(b)

Claim 9

In the action mailed May 6, 2005, claim 9 was rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,970,241 to Deao et al. (hereinafter "Deao").

Claim 9 relates to a method of providing instructions to a processor. As amended, the method includes loading a plurality of instructions into an emulation instruction register from a test interface, receiving a run-test idle state signal, providing the plurality of instructions to the processor in response to the receipt of the run-test idle state signal, and processing the plurality of instructions without receiving another run-test idle state signal. The run-test idle state signal indicates entry of the test interface into a run-test idle state.

Deao describes a microprocessor that includes an emulation unit for debugging the operation of the microprocessor's instruction execution pipeline. In Deao, a "pipe down" procedure is used when the instruction execution pipeline is stopped. The pipe down procedure saves the contents of various registers within the pipeline so that debugging can occur. As part of the pipe down procedure, the fetching of instructions from memory is stopped in response to receipt of a signal indicating that the processor pipeline has halted.

The PTO rejects claim 9 on two different, alternative bases. The first basis asserts that the absence of signal indicating that the processor pipeline has halted (herein the "halt signal") constitutes a run-test idle state signal within the meaning of claim 9. The second basis asserts that a first signal indicative of a pending halt (herein the "pending halt signal") constitutes a run-test idle state signal within the meaning of claim 9.

Applicant respectfully disagrees with both bases of the rejection. In particular, neither the absence of a halt signal nor a pending halt signal is in itself a run-test idle state signal, since neither indicates entry of a test interface into a run-test idle state. In Deao, the absence of a halt signal indicates that the processor pipeline is currently active. The pending halt signal indicates that a processor pipeline halt is

pending. *Neither indicates an idle state, much less an idle state of a test interface.*

Accordingly, Applicant submits that claim 9, and the claims dependent therefrom, are patentable over Deao.

Claim 16

Claim 16 was rejected under 35 U.S.C. § 102(b) as anticipated by Deao.

As amended, claim 16 relates to a processor that includes a test interface, an emulation instruction register adapted to store a plurality of emulation instructions received from the test interface, emulation control logic adapted to supply the plurality of emulation instructions to a processor pipeline in response to detection of a single entry of the test interface into run-test idle state, and a decoder to receive the plurality of instructions for processing.

The rejection of former claim 16 relied upon the contention that the halting of a pipeline constitutes the control of a flow of a plurality of emulation instructions. However, the halting of a pipeline does not constitute the supply of a plurality of emulation instructions in response to detection of a single *entry of the test interface into run-test idle state*, as now claimed.

Accordingly, Applicant submits that claim 16, and the claims dependent therefrom, are patentable over Deao.

Claim 21

Claim 21 was rejected under 35 U.S.C. § 102(b) as anticipated by Deao.

Claim 21 relates to an apparatus that includes operating instructions residing on a machine-readable storage medium. The operating instructions are for use in a device to handle a plurality of emulation instructions. As amended, the operating instructions cause the device to load the plurality of emulation instructions into a single emulation instruction register, have a test interface enter a run-test idle state, provide the plurality of emulation instructions to a processor in response to entry of the test interface into the run-test idle state, and process the plurality of emulation instructions.

The rejection of claim 21 offers no basis for supporting the contention that Deao's instructions are provided in response to entry of the test interface into a run-test idle state. As discussed in the response filed February 10, 2005, when Deao's instruction execution pipeline is stopped, Deao's system executes a pipe down procedure in which the fetching of instructions from memory is stopped. Such a stoppage of the flow of instructions neither describes nor suggests the provision of emulation instructions in response to entry of the test interface into a run-test idle state.

Please note that the two bases relied upon in maintaining the rejection of claim 9 are inapplicable to claim 21. In particular, claim 21 does not recite a run-test idle state signal, but rather deals with a response to entry of the test interface into the run-test idle state.

If the rejection of claim 21 is maintained, Applicant respectfully requests that the basis for the contention that Deao's instructions are provided in response to entry of a test interface into a run-test idle state be identified.

Applicant submits that claim 21, and the claims dependent therefrom, are patentable over Deao.

Rejections under 35 U.S.C. § 103(a)

Claim 1

Claim 1 was rejected under 35 U.S.C. § 103(a) as obvious over Deao and U.S. Patent No. 5,848,288 to O'Connor (hereinafter "O'Connor").

As amended, claim 1 relates to a method that includes receiving a plurality of instructions from a test interface, loading the plurality of instructions into an emulation instruction register, receiving a plurality of instructions from the emulation instruction register, determining a validity of a first instruction of the plurality of instructions by reading width bits in the first emulation instruction, providing the first instruction to a decoder of the processor if the first

instruction is valid, without receiving a run-test idle state signal, determining a validity of a second instruction of the plurality of instructions by reading width bits in the second instruction, and providing the second instruction to the decoder if the second instruction is valid. Read width bits define the validity and size of the first and second emulation instructions.

The rejection of claim 1 contends that because certain of O'Connor's instructions are not to be immediately executed, they are invalid. Applicant respectfully disagrees. Indeed, O'Connor describes the exact opposite, i.e., that instructions after an end of bundle are valid and issuance is simply delayed. *See, e.g.*, col. 3, line 41-46 (describing that instruction B issues despite being found after an end of bundle).

Thus, O'Connor only uses an end of bundle bit to prevent the premature issuance of instructions. The validity of the instructions- either before or after the bit- is not checked by reading O'Connor's end of bundle bit.

Please note that the determination of the validity of an instruction by reading width bits was recited in claim 1. Nevertheless, to advance prosecution, Claim 1 has been amended to recite that the read width bits define the validity and size of the first and the second emulation instructions.

Attorney's Docket No.:10559-286001

Applicant asks that all claims be allowed. No fees are believed due at this time. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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